

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended): A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, said information array sharing a read circuit with a main memory array comprising said non-volatile memory; [[and,]]

enabling an error correction coding circuit separate from said information array during reading of said repairing data including corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read;

providing a plurality of columns and rows associated with said non-volatile memory;

associating each of said plurality of columns associated with said non-volatile memory with a respective I/O terminal; and

using a (16,11) Hamming code to associate at least one spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal.

2. (previously presented): The method of claim 1 further comprising the step of:
enabling said error correction coding circuit during an access of said main
memory array comprising said non-volatile memory for correcting a
correctable error if a particular address corresponds to an address of at
least one defective column comprising said main memory array.

3. (previously presented): The method of claim 2 wherein said particular address
comprises a Y-address corresponding to said at least one defective column.

4. (previously presented): The method of claim 1 further comprising the step of:
using a read circuit linked to said main memory array to read data from said main
memory array and to transmit the read data to said error correction coding
circuit;
said error control circuit being connected to said volatile latch array to permit data
to be transferred from said error correction coding circuit to said volatile
latch array;
said error correction coding circuit being linked a decoder circuit and thereby to
said information array, at least one spare row and said main memory
array, and wherein said main memory array includes a normal array and
at least one spare column.

5. (previously presented): The method of claim 4 wherein said volatile latch array is linked to said decoder circuit to thereby permit data contained within said volatile latch array to be accessed by said decoder circuit.

6. (previously presented): The method of claim 1 further where in the step of reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory further comprises the steps of:

accessing said repairing data contained within said information array following initialization of a computer system associated with said non-volatile memory; and thereafter transferring said repairing data to said volatile latch array.

7-10 (canceled)

11. (currently amended): A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a reading circuit for reading repairing data from an information array associated with said non-volatile memory to a volatile latch array associated with said non-volatile memory, said information array sharing said read circuit with a main memory array comprising said non-volatile memory; [[and,]] an error correction coding circuit separate from said information array adapted to be enabled during reading of said repairing data including reading

corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read;

a plurality of columns and rows each associated with said non-volatile memory, wherein each of said plurality of associated columns and rows is further associated with a respective I/O terminal; and
a spare column, wherein said error correction coding circuit using a (16,11) Hamming code to associate said spare column with at least two of each of said plurality of columns associated with both said non-volatile memory and with a respective I/O terminal.

12. (currently amended): The system of claim 11 wherein:

said error correction coding circuit is adapted to be enabled during an access of
[[a]] said main memory array comprising said non-volatile memory for correcting a correctable error if a particular address corresponds to an address of at least one defective column.

13. (previously presented): The system of claim 12 wherein said particular address comprises a Y-address corresponding to said at least one defective column.

14. (currently amended): The system of claim 11 further wherein
said read circuit is linked to said main memory array to thereby permit data to be
read from said main memory array and to be transmitted to said error
correction coding circuit;
said error control circuit is connected to said volatile latch array to thereby permit
data to be transferred from said error correction coding circuit to said
volatile latch array; and
said error correction coding circuit is linked to a decoder circuit, and thereby to
said information array, at least one spare row, and said main memory
array, said main memory array includes a normal array and at least one
spare column.

15. (previously presented): The system of claim 14 further wherein said volatile
latch array is linked to said decoder circuit to thereby permit data contained within said
volatile latch array to be accessed by said decoder circuit.

16. (previously presented): The system of claim 11 wherein:
said repairing data contained within said information array is accessed following
initialization of a computer system associated with said volatile latch
array, thereby resulting in the transfer of said repairing data to said
volatile latch array.

17-22. (canceled)

23. (previously presented): The method of claim 1 further comprising the step of:
enabling the error correction coding circuit unconditionally when accessing an
information row within said information array to make certain that said
repairing data will be correctly obtained.

24-25. (canceled)